Attorney Docket SEL 171

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)
Masaya Kadono et al.	)
Serial No.: 09/535,233	)
Filed: March 24, 2000	)
For: A Method Of Manufacturing A Semiconductor Device	)
Art Unit: 2823	)
Confirmation No.: 1670	)
Examiner: W. Coleman	)

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE (L) TO FINAL REJECTION

Sir:

Applicants have the following response to the Final Rejection of August 1, 2006.

Applicants appreciate the Examiner's allowance of Claims 37-42.

Applicants will address each of the Examiner's remaining rejections in the order in which they appear in the Final Rejection.

Claim Rejections - 35 USC §102

Claims 11-18, 23-32 and 34-35

In the Final Rejection, the Examiner continues to reject Claims 11-18, 23-32 and 34-35 under 35 USC §102(b) as being anticipated by Konuma (US 6,127,279). This rejection is respectfully

traversed.

More specifically, the Examiner appears to admit that Konuma does not specifically teach forming a semiconductor island by spin etching. The Examiner states that Konuma teaches forming a gate electrode (106) by spin etching (and cites col. 7, lines 8-14 in Konuma). The Examiner then contends that "[t]he Examiner believes that Konuma would suggest forming the silicon island by spin etching because Konuma teaches that it is possible to uniformly apply a solution to a substrate on which a resist is formed by ultraviolet light irradiation or ozone water contact to the surface of the resist because, to decrease a contact angel of the solution, in solution applying method in which the moving speed of etching solution over the surface of the substrate is high (column 16, lines 46-52). This would suggest that spin etching can be used not only for the gate electrode but for any film on the substrate as described by Konuma)." Applicants respectfully disagree with the Examiner's conclusion.

Applicants respectfully submit that since Konuma does not teach a method for forming an island-like silicon film (103; See col. 7, lines 4-8), Konuma cannot disclose or suggest the limitation of Claims 11 and 15 of applying etching solution to a surface of the semiconductor island.[1] Therefore, Konuma cannot anticipate the method of independent Claims 11 and 15 of the present application.

Accordingly, it is respectfully submitted that independent Claims 11 and 15 and those claims dependent thereon are not anticipated by Konuma.

With regard to independent Claims 23 and 27, the Examiner contends that "since Konuma teaches the fabrication of various semiconductor devices, the wiring layer is inherent." Applicants

[1] Applicants note that while Konuma appears to teach applying a solution containing nickel to introduce nickel into the amorphous silicon film at col. 15, lines 1-3, it appears that the solution containing nickel is not for etching or an etching solution.

respectfully disagree. Konuma does not appear to disclose or suggest the claimed feature of forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces, as recited in Claims 23 and 27, and there has been no showing as to how Konuma discloses this feature. Accordingly, it is respectfully submitted that independent Claims 23 and 27 and those claims dependent thereon are not anticipated by Konuma.

For at least the above-stated reasons, it is respectfully requested that this anticipation rejection be withdrawn.

Claims 19-22 and 36

The Examiner also rejects Claims 19-22 and 36 under 35 USC §102(b) as being anticipated by Chiyou et al. (JP 11-016866). This rejection is also respectfully traversed.

With regard to Claim 19, the Examiner appears to be making the following assertions regarding the claimed features of Claim 19:

"forming a patterned resist mask over said crystallized semiconductor film" is *well known*;

"patterning the crystallized semiconductor film to form at least one semiconductor island over said substrate" is *inherent*;

"removing the patterned resist mask located over said semiconductor island" is a *necessary requirement* to make functional devices; and

that the formation of a gate insulating film and a gate electrode are *well known* to be incorporated in the devices taught by Chiyou.

Applicants respectfully submit that this is not a proper finding for an anticipation rejection of showing each and every claimed element in a reference. Therefore, this 102(b) rejection is improper.

Additionally, the Examiner contends that Chiyou discloses the claimed features of "crystallizing

said semiconductor film" at [0052] and "spinning the substrate [0051] after removing the patterned resist mask." However, Chiyou teaches a spin desiccation for desiccate (drying) a substrate after removal of the natural oxidation film 4. See [0050] - [0053] in Chiyou. Hence, Chiyou does not disclose or suggest the claimed features of "spinning the substrate after removing the patterned resist mask;" and "applying an etching solution to a surface of said semiconductor island and scattering the etching solution *during said spinning*" (emphasis added).

Furthermore, Claim 19 clearly recites an order for the claimed steps:

[a] crystallizing said semiconductor film;

[b] forming a patterned resist mask over said *crystallized semiconductor film* [hence, the semiconductor film must be crystallized];

[c] patterning the *crystallized semiconductor film* to form at least one semiconductor island *over* said substrate;

[d] removing the patterned resist mask located over *said semiconductor island*; [hence, the semiconductor island must be formed]

[e] spinning the substrate [over which the semiconductor island is formed in [c] above] *after* removing the patterned resist mask; [hence, the patterned mask must be formed before it is removed (bracketed matter and emphasis added for illustration purposes].

Accordingly, a feature of the claimed invention is spinning the substrate over which the crystallized semiconductor island has been formed.

In contrast, Chiyou's process (i.e. the spin desiccation) in [0051] is pretreatment for the laser crystallization in [0052]. Hence, Chiyou does not disclose or suggest spinning the substrate after crystallization as in the claimed method, and therefore Chiyou cannot disclose or suggest the method of independent Claim 19 or those claims dependent thereon.

The Examiner also contends that Chiyou discloses a semiconductor island in Drawing 3. As Applicants previously explained, Drawing 3 does not teach or suggest that the silicon (of a "Surface of Silicon" in Drawings 3A and 3B) is patterned into a semiconductor island in Drawings 3A and 3B and paragraphs [0008] and [0009].

In order to make this clear, Applicants have prepared and attached a translation of Drawings 3A and 3B. This clearly shows evidence of a water drop and a silicon oxide (water mark), and confirms that neither Drawings 3A or 3B show a semiconductor island. Further, neither drawing shows that silicon is patterned into a semiconductor island.

Accordingly, for at least the above-identified reasons, it is respectfully submitted that independent Claim 19 and those claims dependent thereon are not anticipated by Chiyou, and it is respectfully requested that this rejection be withdrawn.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

Please charge Deposit Account No. 50-1039 for any fee due for this response.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: November 1, 2006

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English Translation of
Drawings 3A and 3B of
Chiyou et al. (JP 11-016866)

[Drawing 3]